**PART 2.** **Study the datasheet of 74HC138D and tell what is the purpose of using it with 7 segments**

**displays.**

**DESCRIPTION: -**

• 3-to-8 Line Decoder

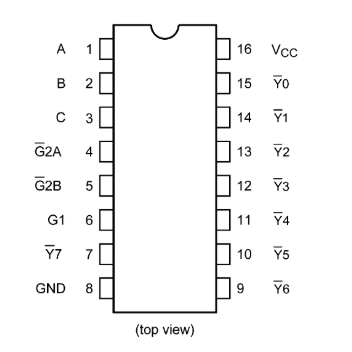
The 74HC138D is a high-speed CMOS 3-to-8 DECODER fabricated with silicon gate C 2MOS technology. It achieves the high-speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs (Y0 - Y7) will go low. When enable input G1 is held low or either G2A or G2B is held high, decoding function is inhibited and all outputs go high. G1, G2A, and G2B inputs are provided to ease cascade connection and for use as an address decoder for memory systems. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**Features**

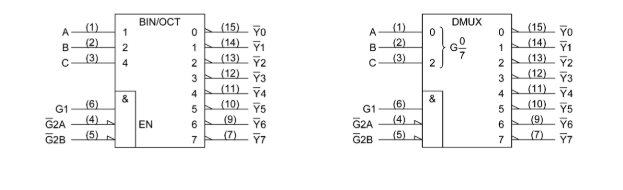
1) High speed: tpd = 16 ns (typ.) at VCC = 5 V (2) Low power dissipation: ICC = 4.0 µA (max) at T a = 25 V

(3) Balanced propagation delays: tPLH ≈ tPHL (4) Wide operating voltage range: VCC(opr) = 2.0 to 6.0 VApplications  
• Memory chip select decoding  
• Demultiplexing  
• Single line peripheral control  
• Allow simple serial bit streams from a microcontroller to control as  
many peripheral lines as needed

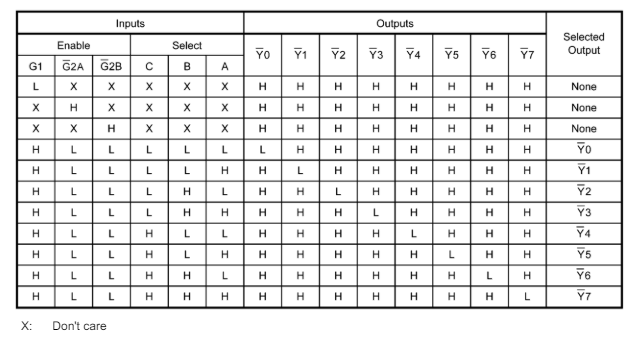
**PIN ASSIGNMENT: -**



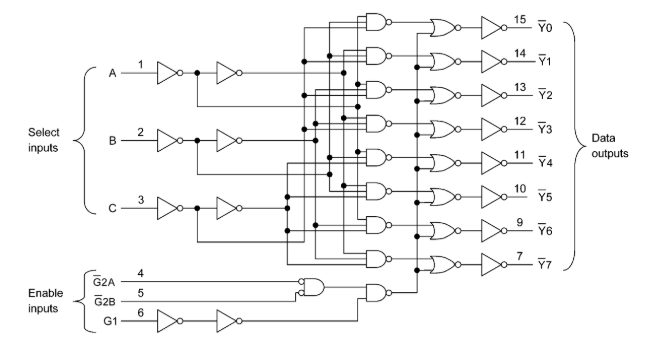
**IEC LOGIC SYMBOL: -**



**TRUTH TABLE: -**

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**LOGIC DIAGRAM: -**

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